Code No: 124AF **R15**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year II Semester Examinations, September/October - 2023

DIGITAL DESIGN USING VERILOG HDL

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART - A

(25 Marks)

1.a)	Write about system tasks.	[2]
b)	Define scalars and vectors.	[3]
c)	Define tri-gate state.	[2]
d)	What is continuous assignment structure?	[3]
e)	Write about Repeat construct.	[2]
f)	Draw a simulation flow chart.	[3]
g)	Write about Bi Directional Gates.	[2]
h)	Mention the significance of module parameters.	[3]
i)	What is feedback model?	[2]
j)	Write a short note on design verification.	[3]

PART - B

(50 Marks)

2.a)	What are the different levels of design description? Explain.	
b)	What are the functions of Programming Language Interface (PLI)? Explain.	[5+5]
	OR	
3.	Explain in detail about the concepts of numbers and strings with suitable examples.	[10]
4.a)	Write a Verilog program in gate level for 3 to 8 decoder.	
b)	Write about array of instances of primitives.	[5+5]
	OR	
5.a)	Write a Verilog module for J K flip-flop using NAND gates.	
b)	Write a short notes on strengths and construction.	[5+5]
6.a)	Design a counter module and test bench to illustrate the use of WAIT.	
b)	Differentiate between a sequential block and a parallel block.	[5+5]
	OR	
7.a)	Write a Verilog code using case statement for any one example.	
b)	What is the difference between an Intra statement delay and an Inter statement delay? Explain.	[5+5]

8.a) Write the code for CMOS switch of parallel combination.

b) Discuss the basic transistor switches. [5+5]

OR

9.a) Explain the different types of user defined primitives with examples.

b) Write short notes on the computer directives. [5+5]

10. Explain capacitive model of a sequential circuit and compare it with other models.[10]

OR

11.a) How the memory initialization carried out in Verilog? Explain with an example.

b) Write the Verilog code for basic functional unit of a dynamic shift register. [5+5]

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